

IN THE CLAIMS:

Please add claims 27-29 as follows:

27. (new) A method for manufacturing a semiconductor device, the method comprising:

- forming a gate dielectric layer on a silicon substrate;
- forming a first conductive layer on the gate dielectric layer;
- forming a first upper layer comprising a silicon nitride layer on the first conductive layer;
- forming a second upper layer comprising a polysilicon layer on the first upper layer,

wherein the first upper layer is positioned between the first conductive layer and the second upper layer;

- patterning and etching the first conductive layer, the first upper layer and the second upper layer so that the first conductive layer, the first upper layer and the second upper layer all have an identical width defined by side end surfaces;
- after the patterning and etching, forming sidewall spacers on the side end surfaces of the first upper conductive layer, the first upper layer and the second upper layer;
- after the forming sidewall spacers, forming an insulation layer over the second upper layer and the sidewall spacers;
- planarizing the insulation layer until an upper surface of the second upper layer is exposed;
- after the planarizing, removing the second upper layer and removing the first upper layer from between the sidewall spacers, while at least part of the first conductive layer remains between the sidewall spacers, wherein the removing the second upper layer and the removing the first upper layer forms an opening between the sidewall spacers; and
- forming a second conductive layer in the opening between the sidewall spacers to form a gate electrode that includes at least the first conductive layer and the second conductive layer.

28. (new) A method as in claim 27, further comprising forming the first conductive layer from a material comprising polysilicon, forming the first upper layer from a material

comprising silicon nitride, and forming the second upper layer from a material comprising polysilicon.

29. (new) A method as in claim 27, further comprising, after the removing the second upper layer and removing the first upper layer from between the sidewall spacers, and prior to the forming a second conductive layer in the opening, forming a barrier layer in the opening so that the barrier layer is in direct contact with the first conductive layer and an interior surface of the sidewall spacers.